WHAT IS CLAIMED IS:

1. A system for interfacing in an open system interconnection type network, said system comprising:

a media access control layer configured to manage data flow over said open system interconnection type network;

a physical layer configured to code data for transmission to a medium;

an eight bit transmit data bus configured to enable data transfer from said media access control layer to said physical layer, wherein said eight bit transmit data bus is driven by said media access control layer;

an eight bit receive data bus configured to enable data transfer from said physical layer to said media access control layer, wherein said eight bit receive data bus is driven by said physical layer;

a transmit ON signal bus configured to indicate to said physical layer that a data frame is available on said eight bit transmit data bus and to indicate a request by said media access control layer for said physical layer to apply a backoff signal; and

a receive ON signal bus configured to indicate that to said media access layer valid data is available on said eight bit receive data bus and to indicate that a backoff signal request is received.

2. The system of Claim 1, wherein said eight bit transmit data bus is further configured to enable direct memory access (DMA) from a digital signal processor (DSP), wherein said DSP implements a programmable digital signal processing function of said physical layer.

3. The system of Claim 1, wherein said eight bit receive data bus is further configured to enable direct memory access (DMA) to a digital signal processor (DSP), wherein said DSP implements a programmable digital signal processing function of said physical layer.

4. The system of Claim 1, wherein said media access control layer request said backoff signal upon detection of a collision condition.

5. The system of Claim 1 further comprising a transmit HPNA mode signal bus configured to indicate that a HPNA 1.0 type data frame is available for transmission on said eight bit transmit data bus.

6. The system of Claim 1 further comprising a receive HPNA mode signal bus configured to indicate that a HPNA 1.0 type data frame is available for transmission on said eight bit receive data bus.

7. The system of Claim 1, wherein said backoff signal comprises a HPNA type backoff signal.

8. The system of Claim 1 further comprising a register set configured for managing data signal exchange between said media access control layer and physical layer.

9. The system of Claim 8, wherein a first portion of said register set is implemented in said media access control layer and a second portion of said register set is implemented in said physical layer.

10. The system of Claim 1 further comprising:

a backoff signal slot ON data bus configured to indicate a start of a backoff signal slot;

a transmit enable data bus configured to indicate that a new data frame can be placed on said eight bit transmit data bus;

a reference clock sourced by said physical layer;

a carrier sense signal bus configured to indicate idle and non-idle conditions on transmit and receive mediums;

a collision detection signal bus configured to indicate a collision condition on said transmit and receive mediums;

a receive error signal data bus configured to indicate an error detection in a transmit data frame; and

a receive enable data bus configured to indicate placement of new data on said eight bit receive data bus.

11. A media interface for data exchange between a media access control layer and a physical layer in an open system interconnection layered type network, said media interface comprising:

an eight bit transmit data bus configured to enable data transfer from said media access control layer to said physical layer, wherein said eight bit transmit data bus is driven by said media access control layer;

an eight bit receive data bus configured to enable data transfer from said physical layer to said media access control layer, wherein said eight bit receive data bus is driven by said physical layer;

a transmit ON signal bus configured to indicate to said physical layer that a data frame is available on said eight bit transmit data bus and to indicate a request by said media access control layer for said physical layer to apply a backoff signal; and

a receive ON signal bus configured to indicate to said media access control layer that valid data is available on said eight bit receive data bus and to indicate that a backoff signal request is received.

12. The media interface of Claim 11, wherein said eight bit transmit data bus is further configured to enable direct memory access (DMA) from a digital signal processor (DSP), wherein said DSP implements a programmable digital signal processing function of said physical layer.

13. The media interface of Claim 11, wherein said eight bit receive data bus is further configured to enable direct memory access (DMA) to a digital signal processor (DSP), wherein said DSP implements a programmable digital signal processing function of said physical layer.

14. The media interface of Claim 11, wherein said media access control layer request said backoff signal upon detection of a collision condition.

15. The media interface of Claim 11 further comprising a transmit HPNA mode signal bus configured to indicate that a HPNA 1.0 type data frame is available for transmission on said eight bit transmit data bus.

16. The media interface of Claim 11 further comprising a receive HPNA mode signal bus configured to indicate that a HPNA 1.0 type data frame is available for transmission on said eight bit receive data bus.

17. The media interface of Claim 11, wherein said backoff signal comprises a HPNA type backoff signal.

18. The media interface of Claim 11 further comprising a register set configured for managing data signal exchange between said media access control layer and physical layer.

19. The media interface of Claim 18, wherein a first portion of said register set is implemented in said media access control layer and a second portion of said register set is implemented in said physical layer.

20. The media interface of Claim 11 further comprising:

a backoff signal slot ON data bus configured to indicate a start of a backoff signal slot;

a transmit enable data bus configured to indicate that a new data frame can be placed on said eight bit transmit data bus;

a reference clock sourced by said physical layer;

a carrier sense signal bus configured to indicate idle and non-idle conditions on transmit and receive mediums;

a collision detection signal bus configured to indicate a collision condition on said transmit and receive mediums;

a receive error signal data bus configured to indicate an error detection in a transmit data frame; and

a receive enable data bus configured to indicate placement of new data on said eight bit receive data bus.